PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Takenori OSADA, et al.

Appln. No.: 10/540,513

Confirmation No.: 6641

Filed: June 23, 2005

Docket No: Q88662

Group Art Unit: 2893

Examiner: Eduardo A. RODELA

For: COMPOUND SEMICONDUCTOR EPITAXIAL SUBSTRATE AND METHOD FOR MANUFACTURING THE SAME

DECLARATION UNDER 37 C.F.R. § 1.132

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Takenori Osada, hereby declare and state that I am a citizen of Japan. I graduated from the Third Cluster of Colleges, College of Engineering Science, in the University of Tsukuba in March 1987. I completed the Master's Program in Applied Physics at the University of Tsukuba Graduate School in March 1989.

I worked at Sumitomo Chemical Company, Ltd. beginning in April 1989, and engaged in the study of pigments, electrode materials, polysilane polymer materials, polymer light emitting devices (LED), and compound semiconductor epitaxial substrates. I was also a guest researcher in Linkoping University from October 1996 to December 1997. From May 2006 until the present date, I have worked for Sumika Electronic Materials, Inc. in the United States.

I have reviewed Tanimoto et al. (JP 05-226372) and Kuroda et al. (U.S. Patent No. 5,831,296), which I will refer to as "Tanimoto" and "Kuroda," respectively. I have also reviewed the claims and specification of the above-mentioned application.

The high electron mobility transistor (HEMT) in Kuroda is not the same HEMT disclosed in Tanimoto. Accordingly, the HEMT's in Kuroda and Tanimoto would possess distinct properties. For example, the electron mobility reported in Kuroda's HEMT would not be applicable to the HEMT in Tanimoto. The reason is that Kuroda discloses a HEMT, whereas Tanimoto discloses a strain channel HEMT. A strain channel HEMT has a strain channel layer that is formed by growing a material on a substrate such as GaAs. The material has a different lattice constant from the substrate, but maintains its crystal structure.

This is relevant because the electron mobility of the GaAs layer in the GaAs (strain) channel HEMT in Tanimoto is about 8000 $cm^2/Vsec$ (as described by Tanimoto in Paragraph No. [0004]), whereas the electron mobility of the GaAs layer in the (non-strain) HEMT of Kuroda is 8500 $cm^2/Vsec$. From my review of these references, it is not my understanding that the strain channel HEMT in Tanimoto would have the electron mobility shown in the non-strain channel of Kuroda. Accordingly, I believe that the teachings of Kuroda fail to indicate that the semiconductor layer in Tanimoto would have the electron mobility presently claimed.

With respect to Fig. 6 in Tanimoto, this figure does not disclose that undoped GaAs layers [2] and [4] have a thickness of 2 to 4 nm. Instead, Tanimoto in paragraph [0004] states that:

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"For example, when spacer layer width is not less than 20 nm in the case of GaAs channel layer HEMT, electron mobility becomes about 8000 $cm^2/Vsec$, the maximum value that is attainable by GaAs. However, if spacer layer width is too large, the number of carries produced in a channel will decrease and as a result mutual conductance will also decrease. Usually, the optimum value of spacer layer width was about 2 to 4 nm, at which the electron mobility was 5000 $cm^2/Vsec$."

Accordingly, Paragraph No. [0004] in Tanimoto only explains the defects or problems that existed at the time and which needed to be solved. This passage does not relate to the undoped GaAs layers [2] and [4] in Fig. 6 of Tanimoto.

Further, Tanimoto does not disclose or suggest that the teaching of the spacer layer width provided by the prior art can be applied to the invention within Tanimoto. In fact, this paragraph indicates that when the spacer layer width is as disclosed in the prior art, the electron mobility will be outside of the presently claimed range.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 9/4/09

長田剛規

Takenori OSADA